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A Review Paper on Comparative Evaluation of Carry Select Adder and Modified Carry Select Adder

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Abstract :- In VLSI design system, adders are the Fundamentals blocks. There are various types of adders présent in the system, like full adder, ripple carry adder, carry look ahead adder, carry Save adder, carry select adder etc. They are generally used for airthmatic operation on microprocessor, many data path logic system for Digital signal processor units, and digital computers.Therefore the design of adder play an important role for the efficient implementation of an airthmatic unit.Among all the adders carry select adder is fast ,power efficient but consume more area due to dual RCA structure. The propagation of carry through the adder limit the speed of addition in digital adder. To overcome this problem many approches have been proposed by using Dlatch or binary excess -1 converter instead of ripple carry adder. This technique can be use for n bit carry select adder to reduce the area, delay and power consomption under several criteria.

Keywords:-Binary to excess -1 converter(BEC), D latch ,carry select adder, modified carry select adder, Ripple carry adder.

I. INTRODUCTION

Many arithmetic units, multipliers, FIR filter, DSP processor uses addition as a basic operation. Therefore, design of area, power efficient, high-speed data path logic systems are one of the most substantial areas of research in VLSI system. The performance of adder and integrated circuit depends on efficient design of adder considering all the parameter. There are many types of adder designs are available like Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder having its own advantages and disadvantages. The Ripple carry Adder (RCA) has the most compact design but it is slowest in speed because for an N-bit full adder. Thus,Ripple Carry Adder gives greater delay of all adders for large value of N. To solve the problem of carry propagation delay and to reduce area and power Carry select adder is developed by using dual RCA structure.

To alleviate the problem of carry propagation delay,carry select adder is used in many computational system by generating multiple carries independently and then selecting a carry to generate the sum. However, the conventional carry select uses multiple pairs of Ripple Carry Adders by considering carry input Cin =0 and Cin=1 to generate partial sum and carry and then then the multiplexers (mux) will select final sum and carry, thus it consumes the more area. The basic building block of carry select adder having a pair of ripple carry adder and mux is shown in fig 1.Hence to overcome the problemBinary to Excess-1 Converter (BEC) instead of RCA with Cin=1 is used in the regular CSLA to achieve lower area and power consumption. The main advantage of BEC logic is that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. D latch is also used in conventional carry select adder to achieve lesser delay and area.

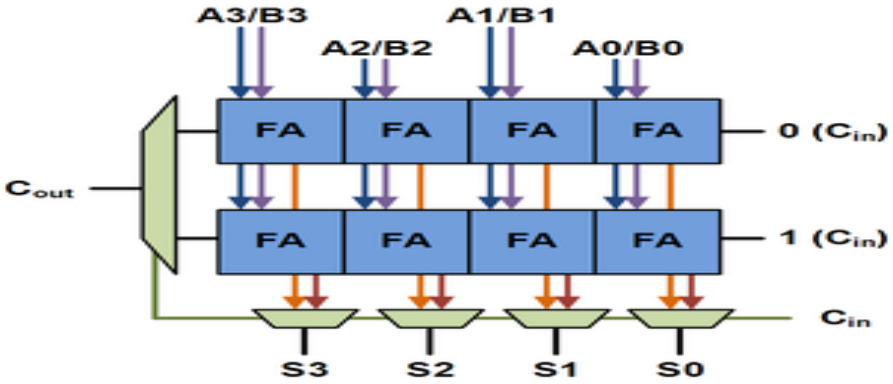

Figure1:-Basic Building Block Carry select adder

II. FAST ADDER

In digital electronics adder is one of the digital circuit that performs number of addition, they can be classified as 1-bit adder to multi bit adder. There are many types of adder where they can be used as to calculate table indices, address and similar operations .The main function of adder is to increase the speed of addition thus by reducing carry propagation time for efficient circuit design. Here we discussed some of the fast adders.

A) Full Adder

A full adder consists of three input often known as A, B, Cin, they are added in row, out three inputs A, B are operands and Cin isabitcarriedinfromthepreviouslesssignificantstage. Figure 2 shows the one-bit full adder. It produces two output, output carry (Cout) and sum.

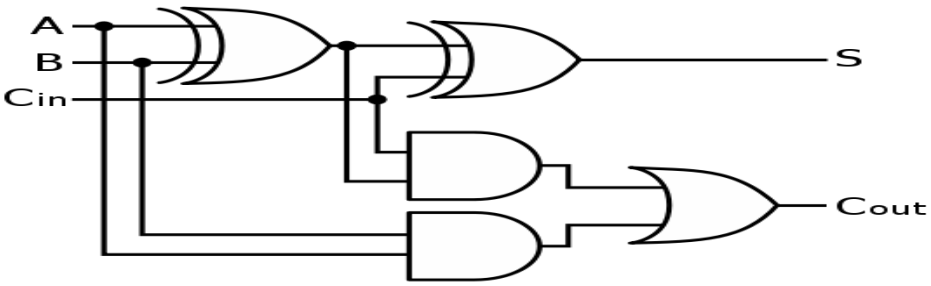

Figure 2: One Bit Full Adder

The output equations are given as follows

Sum =A XOR B (1)

Carry out=(A AND B) + (B AND C) + (A AND C) (2)

B) Ripple carry Adder

An n-bit Ripple Carry Adder (RCA) is a cascaded structure of n full adders. In this carry out of previous full adder is the input carry for the next full adder. As carry ripples from one full adder to the other, it traverses longest critical path and thus gives worst case delay. It calculates sum and carry according to the following equations.Figure 3 shows the ripple carry adder

Si = Ai XOR Bi XOR Ci (3)

Ci+1 = Ai Bi + (Ai + Bi) Ci;where i = 0, 1… n-1 (4)

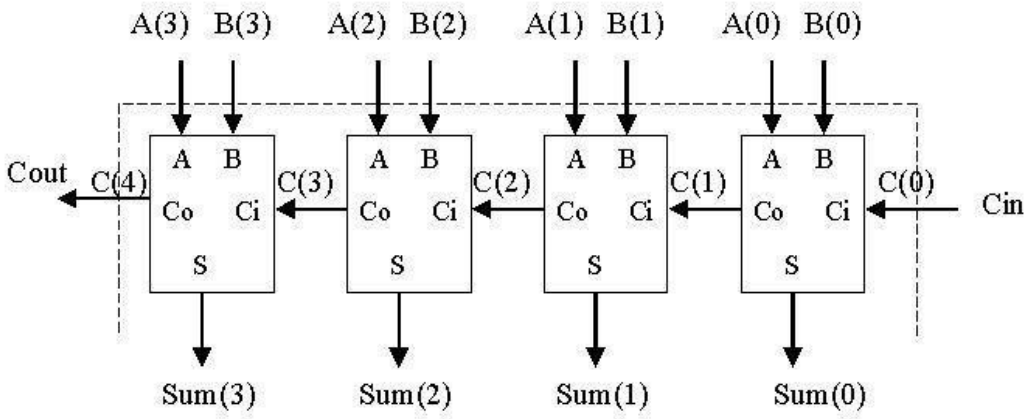

Figure 3(a): Ripple carry adder

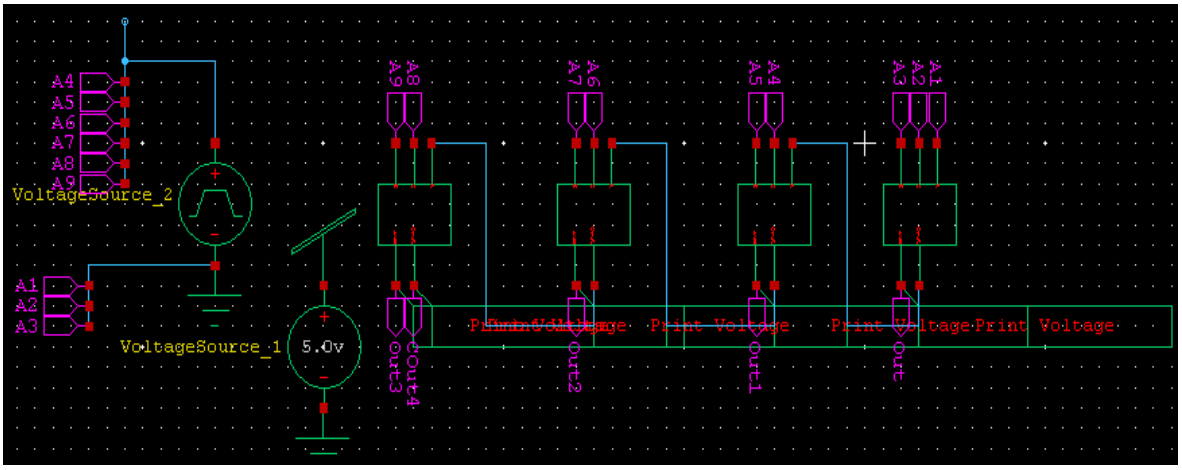

Figure 3(b): RTL schematic of Ripple carry adder

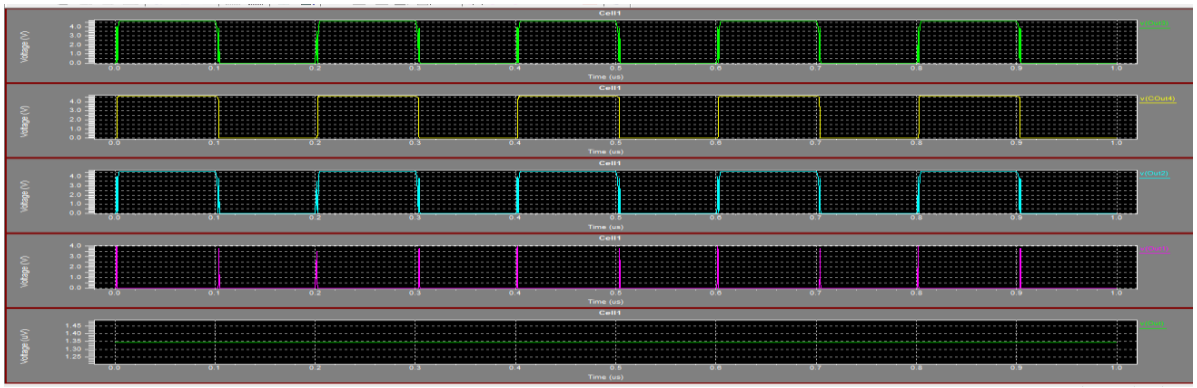

Figure3(c): Simulation of Ripple Carry Adder

RCA is the slowest among all adders but it is area efficient. If the implementation of ripple carry adder is done by concatenating N full adders, the delay of such an adder is increases linearly by 2N gate delays from Cin to Cout with increase in number of bits. Block diagram of RCA is shown in figure above.

C) Carry Select Adder

The carry select adder comes under the category of conditional sum adder. The final sum and carry are calculated by considering input carry as Cin =1 and Cin =0. The final value of sum and carry are selected by

multiplexer. The conventional carry select adder consists two adders for least significant bit and most significant bits that is k/2bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits two k/bit adders. In MSB adders one adder is considered for carry input as one for performing addition and another for carry input as zero. The calculated carry out from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum by multiplexer. Thus adder is divided into stages which increases the area utilization but addition operation become fast. The block diagram of conventional k bit adder is shown in figure4.

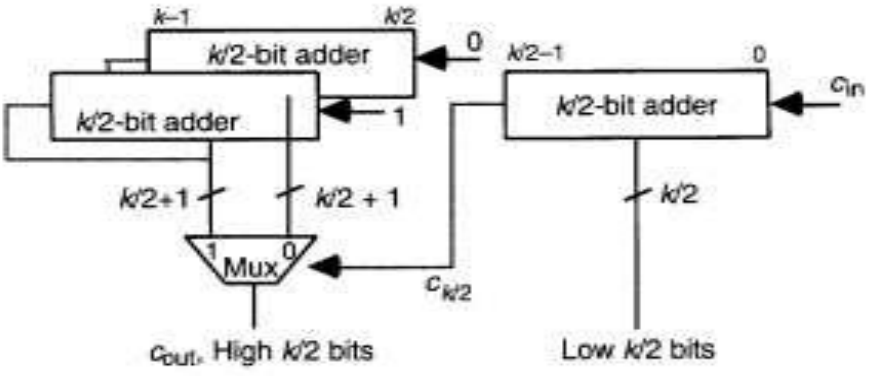

Figure 4(a): block diagram of k-bit adder

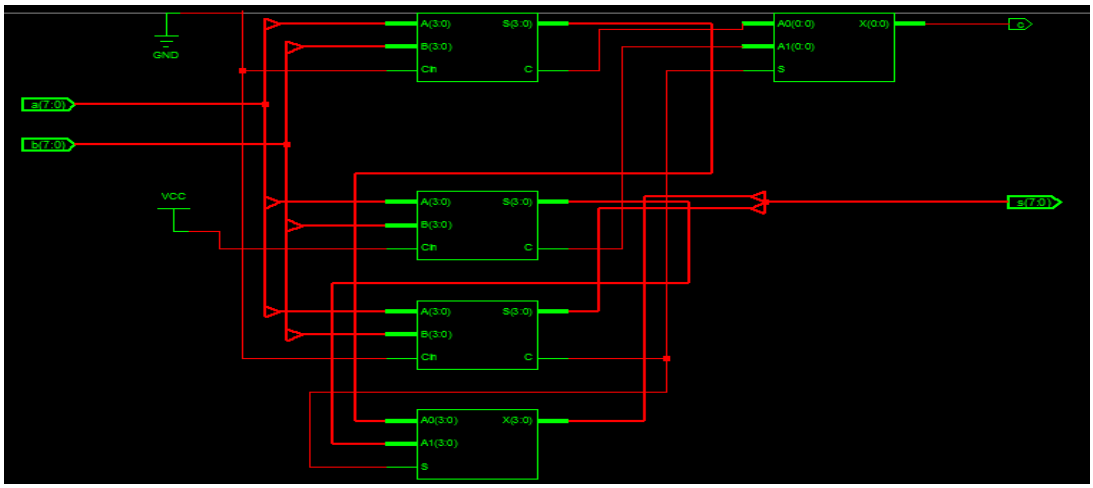

Figure4 (b); RTL Schematic of 8 bit carry select adder

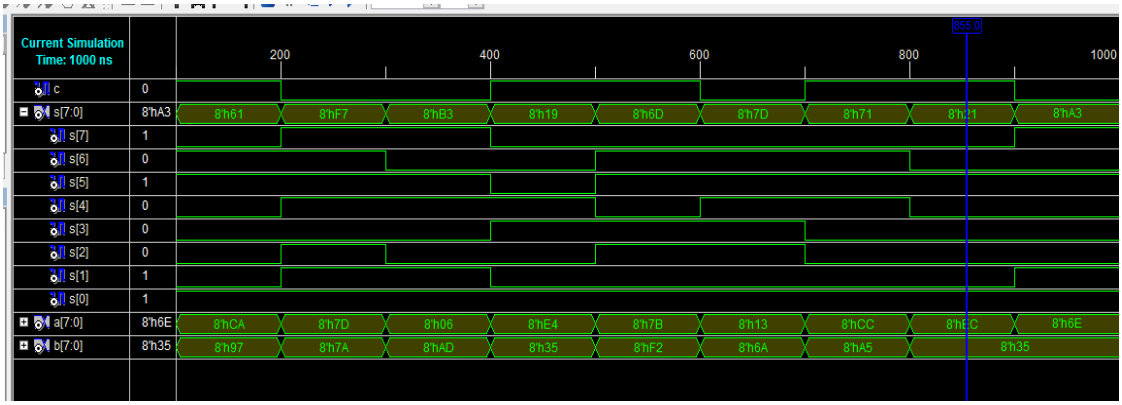

Figure 4(c): Waveform of carry select adder

However, the regular carry select adder is not area efficient because it uses multiple pairs of ripple carry adder. This ripple carry adder is used to generate partial sum and carry by allowing carry input and then the final sum and carry are selectively chosen by the multiplexers.Due to this structure of carry select adder with use of two independent ripple carry adder the overall area of the design increases which leads to an increase in delay. To overcome the above problem, a number of different techniques have been developed to reduce the delay, area and power consumption in the regular carry select adder

III. LITERATURE SURVEY

[1] Ceiang and Hsiao ,in 1998, proposed that,in regular carry select adder instead of using dual structure of ripple adder, an add one circuit is used to replace one carry ripple adder to enhance the area, power and delay.

[2]Ramkumar and Harish, in 2012, propose simple and efficient n new technique at gate level modificationwhich significantly reduce the area and power of square root CSLA.in this technique Binary to Excess-1 converter is used instead ripple carry adder for Cin=1.This improves the speed of addition and thus reduces the area and power consumption.The benefit of BEC logic is that it uses lesser number of logic gates than the single bit full adder structure therefore overall area of structure is reduced.Following figure 5 shows the structure of BEC.

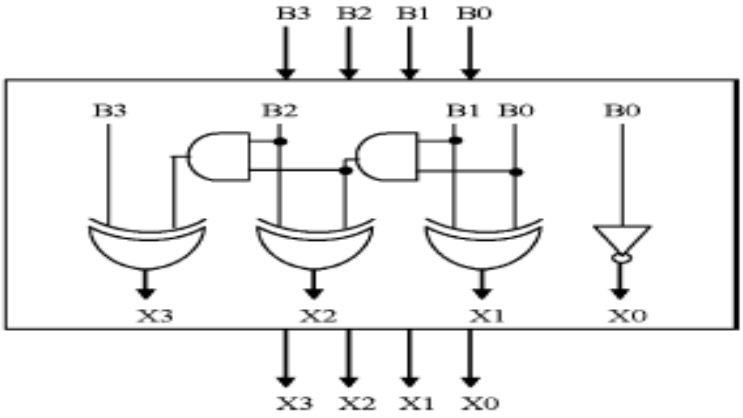

Figure5 (a): Binary to Excess -1 converter

Individual input of the 8:4 multiplexer gets as it input (B3, B2, B1, and B0) and another input of the multiplexer is the BEC output.The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols '~' NOT, '&' AND,'^' XOR)

X0=~B0 (5)
X1=B0^B1 (6)
X2=B2^(B0&B1) (7)
X3=B3^(B0&B1&B2) (8)

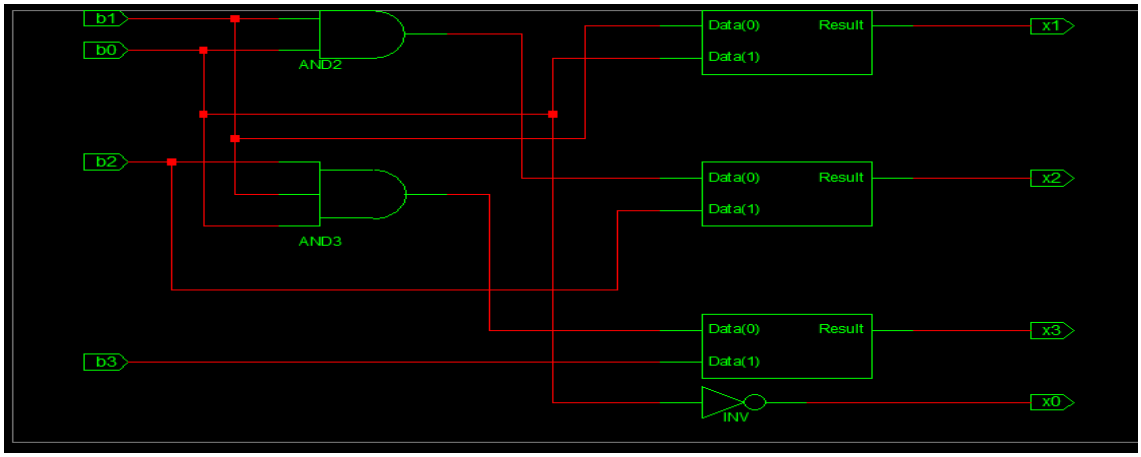

Figure 5(b): RTL schematic of Binary to excess-1 converter

In the modified carry select adder, instead of ripple carry adder for Cin=one, BEC is used .following figure 6 will show the modified carry select adder with BEC.

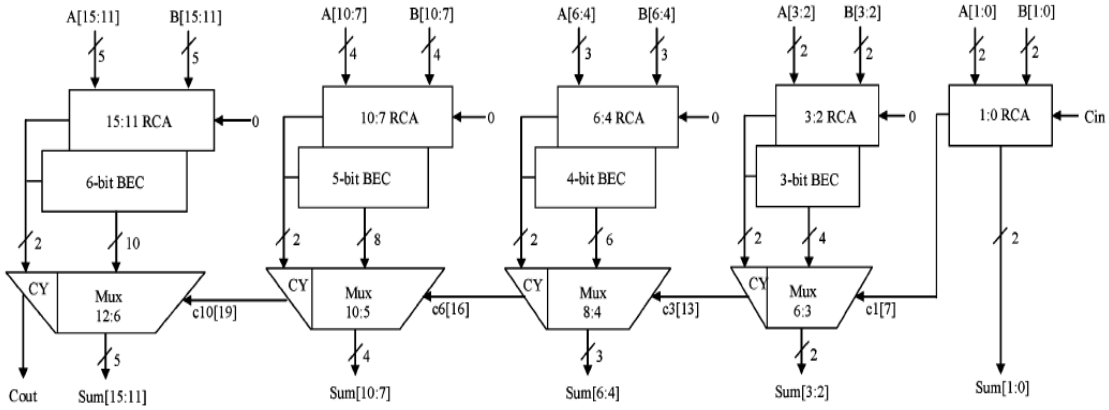

Figure 6: Modified carry select adder with BEC

[3] In 2013,a new design is proposed by Laxman Shanigarapu & Bhavana P. Shrivastava, in which carry select adder is implemented by using D-latch instead of using RCA cascade structure. The main reason behind using DLatch is that it can store the 1-bit information. On applying enable signal, the output of latch is continuously affected by their inputs. In the adder, the addition processfor carry input zero is performedwhen clock signal becomes low means '0'. The main function of the Latch is to accumulate the sum and carry for Cin=1. Figure 7 will show the structure of D latch.

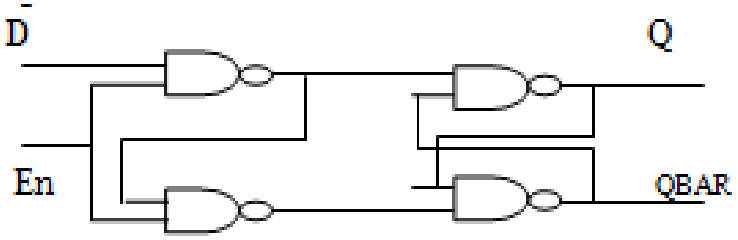

Figure 7: structure of D latch

Initially on applying En=1, the input given to the D latch is output of ripple carry adder and the output of the D-latch follows the input and fed to the multiplexer as an input. When En=0, the last state of the D input is trapped

and held in the latch and therefore the output from ripple carry adder is directly given as an input to the mux without any delay. Now the multiplexer will select s the sum bit according to the input carry(selection bit) and the inputs of the mux are the outputs obtained when en=1 and 0.Following figure 8 will show the carry select adder using D latch.

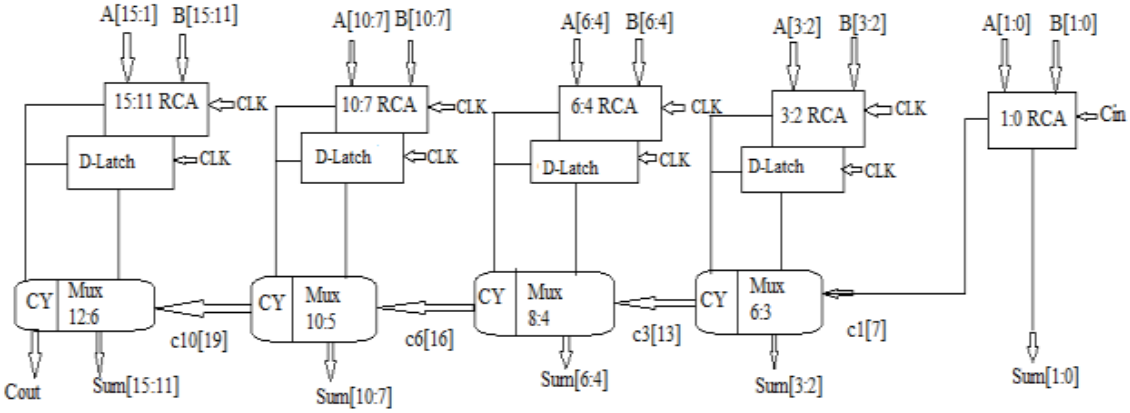

Figure 8: Carry select adder using D-Latch

Table 1 will show the comparison between carry select adder using BEC and D latch

Technique	**No. of slicelut**	**Delay**	**Power consumption**
Csla using RCA	32	10.65 ns	326 mW
Csla using bec-1	40	13.88 ns	302 mW
Csla using Dlatch	48	4.67 ns	277 mW

IV. CONCLUSION

The reduction in the number of gates as stated in this work offers the great advantage for lesser area and reduction in total power consumption. In the all above paper, the design of an area-efficient carry select adder is proposed by different logic. We can reduce the area, delay and power of carry select adder using above techniques andthus there is new change in Cmos technology file.

REFERENCES

Journal Papers:

[1] Ceiang, T. Y. and Hsiao, M. J., (Oct. 1998)*, "Carry-select adder using single ripple carry adder," Electron. Lett. vol. 34, no. 22, pp. 2101– 2103.*

[2] B. Ramkumar and Harish M Kittur, *"Low Power and Area Efficient Carry Select Adder" IEEE Transactions on Very Large Scale Integration (VLSI) systems-2011.*

[3]Laxman Shanigarapu*, Bhavana P. Shrivastava,"*Low-Power and High Speed Carry Select Adder",International Journal of Scientific and Research Publications, Volume 3, Issue 8, August 2013, ISSN 2250-3153.*

[4] Ramkumar, B., Kittur, H.M. and Kannan, P. M., (2010)*, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.*

[5] B. Ramkumar and Harish M Kittur*," Low-Power and Area-Efficient Carry Select Adder", IEEE Transactions on VeryLarge Scale Integration (VLSI) Systems, VOL. 20, NO. 2, February 2012*.

*[6]*Bedrij, O. J., (1962)*, "Carry-select adder," IRE Trans. Electron. Comput. Pp.340–344.*

[7] M.Priyadharshini*, M.Thiruveni*,"Performance Evaluation of Carry Select Adder-Review,"International Journal of Engineering Sciences & ResearchTechnology.ISSN: 2277-9655November 2014.*

*[8]*Amol D. Rewatkar, Prof. Sumit. R. Vaidya, Prof. Rajashree. N. *Mandavgane,"A Review Based on Performance of Carry Select Adder",ISSN: 2393-994X Karpagam Journal Of Engineering Research (KJER) Volume No.: III, Special Issue on IEEE Sponsored International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS'15.*

Books:

[1] Mr.P Raja "*DigitalElectronics*".

*[2]*J. M. Rabaey, *"Digital Integrated Circuits—A Design Perspective*". Upper Saddle River, NJ: Prentice-Hall, 2001.