International Journal of Emerging Trends in Engineering and Basic Sciences (IJEEBS)
ISSN (Online) 2349-6967
Volume 2, Issue 2(Mar-Arp 2015), PP23-30

Design of Phase Locked Loop: CMOS Technological Approach

Prof. G. R. Agrawal[1], Prof. V. M. Dhumal[2]
[1](Deptt. of Electronics Engineering, Govindrao Wanjari College of Engineering & Technology/RTMNU, India)
[2](Deptt. of Electronics Engineering, Priyadarshini J. L. College of Engineering & Technology /RTMNU, India)

Abstract :- The power consumption is an important factor in communication and embedded system applications. The power consumption of any device can be reduced, only when there is reduction in static and dynamic power consumption .The performance of the circuit is also degraded due to minimizing the power supply requirement. This paper reports on the design of a phase-locked-loop (PLL) for on-chip clock generation for a high-performance application. The power consumption of the applications has been reduced by scaling down the supply voltage. The whole system has been implemented using a 12.5um CMOS process that features low-threshold voltages for MOS devices to maintain the speed performance.

Keywords: - Vco, Charge Pump, Frequency Divider, PLL

I. Introduction

The rapid development VLSI Technology prove to be the main factor in the growth achieved in electronic industry .The integrated circuit proved to be the important part of all types of electronic applications, which leads to the rapid industrialization.

The design of the system is being done on Tanner Tool. Tanner Tool provides a complete line of software solution that catalyzes innovation for the design, layout and verification of analog and mixed signal integrated circuits(IC's).The role of oscillators is to create a periodic logic or analog signal with stable and predictable frequency. The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase detector principles.

A PLL is close loop frequency control system based on the phase difference between the clock input signal and feedback clock signal of controlled oscillator. The design of the system is being done on Tanner Tool. Tanner Tool provides a complete line of software solution that catalyzes innovation for the design and verification of analog and mixed signal integrated circuits(IC's). The role of oscillators is to create a periodic logic or analog signal with stable and predictable frequency.

The phase-lock-loop (PLL) is commonly used in microprocessors to generate a clock at high frequency from an external clock at low frequency. The PLL is also used as a clock recovery circuit to generate a clock signal from a series of bit transmitted in serial without synchronization clock.

The PLL uses a high frequency oscillator with varying speed, a counter, a phase detector and a filter. The PLL includes a feedback loop which lines up the output clock ClkOut with the input clock ClkIn through a phase locking stabilization process. When locked, the high input frequency fout is exactly N* fin as shown in figure.1. A

variation of the input frequency fin is transformed by the phase detector into a pulse signal which is converted in turn into variation of the analog signal Vc .This signal changes the VCO frequency.

II. BASIC PHASE LOCKED LOOP

Analog PLLs are generally built of a phase detector, low pass filter and voltage controlled oscillator (VCO) placed in a negative feedback configuration as shown in fig.2. There may be a frequency divider in the feedback path or in the reference path, or both, in order to make the PLL's output clock an integer multiple of the reference. A non-integer multiple of the reference frequency can be created by replacing the simple Divide-by-N counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.

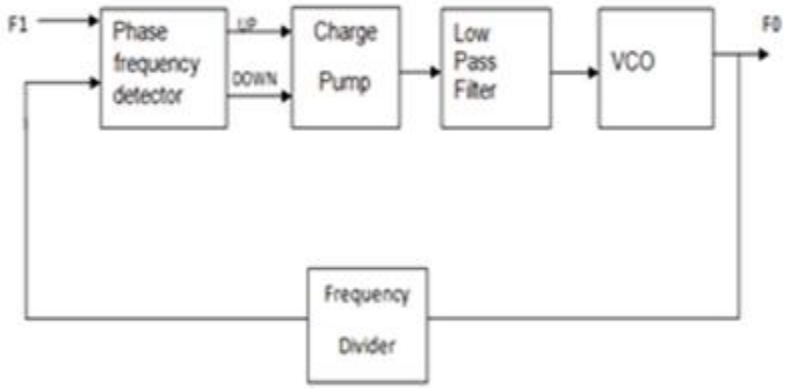

Fig. 1: Basic Phase Locked Loop

The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. Then, if the phase from the oscillator falls behind that of the reference, the phase detector causes the charge pump to change the control voltage, so that the oscillator speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector causes the charge pump to change the control voltage to slow down the oscillator. The low-pass filter smooth out the abrupt control inputs from the charge pump. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs.

Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system. A phase locked loop (PLL) with a single voltage controlled oscillator (VCO) is generally configured to lock multiple internal clocks to multiple incoming data signals of different frequencies. Because of low power scalability with lambda based rules, very high levels of integration and high performance, PLL with low power output is to be implement using 12.5um deep submicron technology of VLSI, have been published but are not well known. Describe new or substantially modified methods, give reasons

for using them and evaluate their limitations. Include number of observations and the statistical significance of the finding when appropriate. Detailed statistical analyses, mathematical derivations, and the like may sometimes be suitably presented in the form of one or more appendices.

III. VOLTAGE CONTROLLED OSCILLATORS

Fig.3 shows the circuit diagram of the VCO cell used in VCO 100.VCO cell 200 includes transistors 221-231 and 222-232 as complementary CMOS inverters and transistor 223-224 and 233-234 as cross coupled transistors. The cross coupled transistors do two things. First, they don't let the inverters 221-231 and 222-232 operate independently, and they keep the timing relationship between the inverters with 180 phase difference. Second, they create extra gain and extra gain and extra phase shift so that the oscillator can oscillate

With only 2 stage .Transistors 221,222,223and 224 are all connected to node 'A' and node 'A' is coupled to Vdd through source follower transistor 203.Voltages Vip and Vin are respectively coupled to inverters 221-231 and 22-232. The outputs are taken from nodes Vop and Von. As the VCOIN moves, node 'A' follows with the same manner with some voltage difference which depends on the type of N transistor used for the source follower and its size and the size of the rest of the transistors and the voltage of VCOIN.

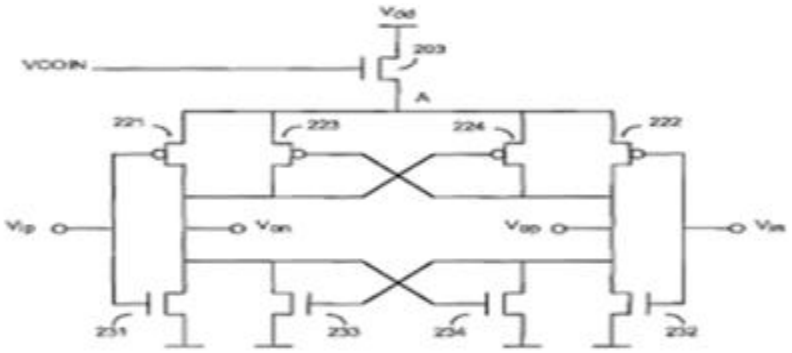

Fig. 2: Voltage Controlled Oscillator

The N transistor in the source follower can also be a native device. Since this complementary inverters with cross coupled transistor has very high gain, even with low voltage at node 'A' this oscillator can oscillate .Therefore, this oscillator can cover a very wide range, and the fact that it is only a 2 stage VCO, it can operate up to a very high frequency. Also the complementary CMOS Architecture with cross-coupled transistors generates sharp-edges while consuming low power. The transistor sizes can be adjusted to get same rise and fall time, and consequently a symmetrical waveform which reduces the phase noise. The source follower will isolate vdd from node 'A' so it reduces the PSS.

IV. PHASE- FREQUENCY DETECTOR

The proposed solution is shown in Fig.4. It is a phase frequency detector with a short duration of the reset path adopted from [5]. PFD operation is the same as in a standard detector [6], but implementation is close to dynamic flip-flop in TSPC logic. The resetting module has been implemented differently in relation to the conventional method. When both signals (up and down) are in the high state then the reset is started, but the slave part has an asynchronous reset and the master part is resetting synchronously. PFD is completely symmetrical, there is no division in its construction between the master and the slave block, the master block is chosen when first upcoming signal appears. Synchronous reset in PFD increases the maximum operating frequency and significantly reduces power consumption. In [5] a slight increase of the maximum.

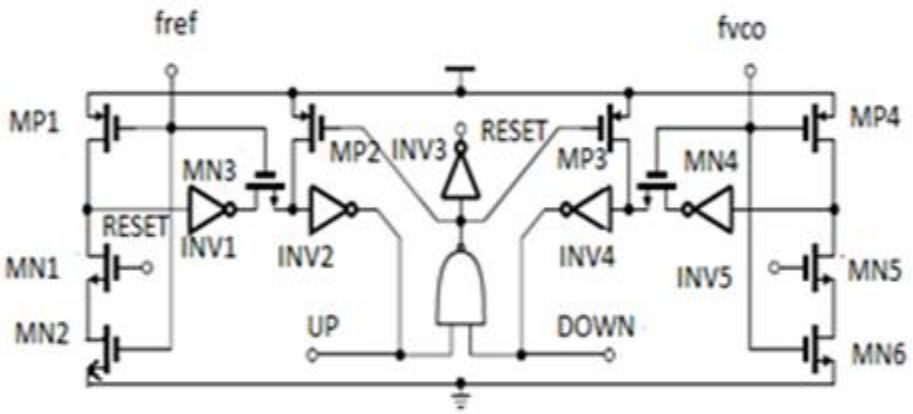

Fig. 3: Phase Frequency Detector

Frequency was achieved, but for the project presented in this paper it is not so important because of the relatively low frequency for PFD (125 MHz). This design also reduced by half the power consumption compared to conventional PFD, which was a reason to use concepts from this circuit.

V. PMOS GATE-CONTROLLED VOLTAGE DOUBLER

To reduce both conduction loss and reversion loss, another voltage doubler design

was reported in [7], with a So-called PMOS gate control. As illustrated in Fig. 5, an NMOS pair, Mna and Mnb, are driven by control signals Vb and Va, respectively. In the meanwhile, a PMOS pair, Mpa and Mpb, are driven by the control signals Vga and Vgb, respectively. To reduce the reversion loss, in Phase A (B), the voltage Va (Vb) should reach 2Vdd before the PMOS transistor, Mpa (Mpa) is turned on; and Va should remain at 2Vdd until Mpa (Mpb) is

turned off. Similarly, the voltage Vb (Va) should drop to Vdd before the NMOS transistor, Mnb (Mna), is turned on. Meanwhile, Vb (Va) should remain at Vdd until Mnb (Mna) is turned off.

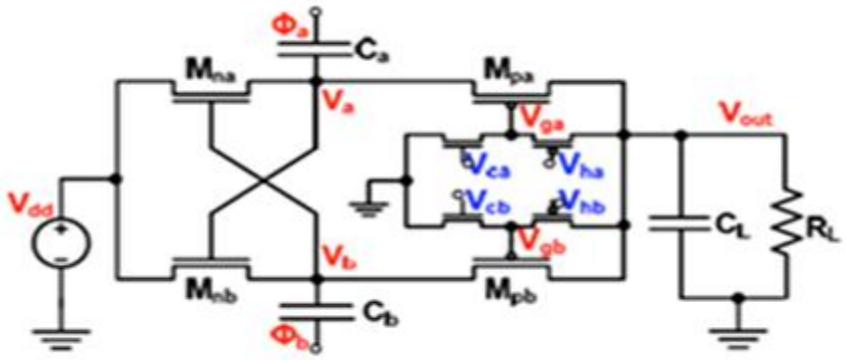

Fig. 4: PMOS Gate Controlled Voltage Doubler

The Voltage swings of Vga and Vgb need to be set to 2Vdd. In Addition, the 2Vdd gate-drive voltages at Mpa and Mpb also reduce the conduction loss. To eliminate leakage current, Vga is charged to 2Vdd before Va starts to drop. However, the four gate control signals all require buffers to drive the power stage, leading to extra power penalty. Meanwhile, Vga and Vgb need to be directly powered by the output Vout (equal to 2Vdd), which increases the switching power loss of buffer drives, level shifters and the power switches.

VI. FREQUENCY DIVIDER

The frequency divider consists of three D-type flip flops in modulo 2 configurations in TSPC logic adopted from [8]. A single stage, divide by 2 circuits, is shown in Fig.6.

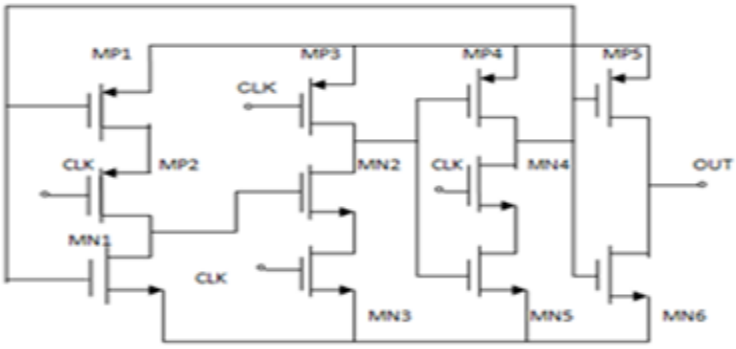

Fig. 5: Frequency Divider

In relation to the solution presented in the publication [8] inverter is added to the output to improve the slew rate (transistors MP5, MN6).

VII. RESULTS

Results of particular blocks

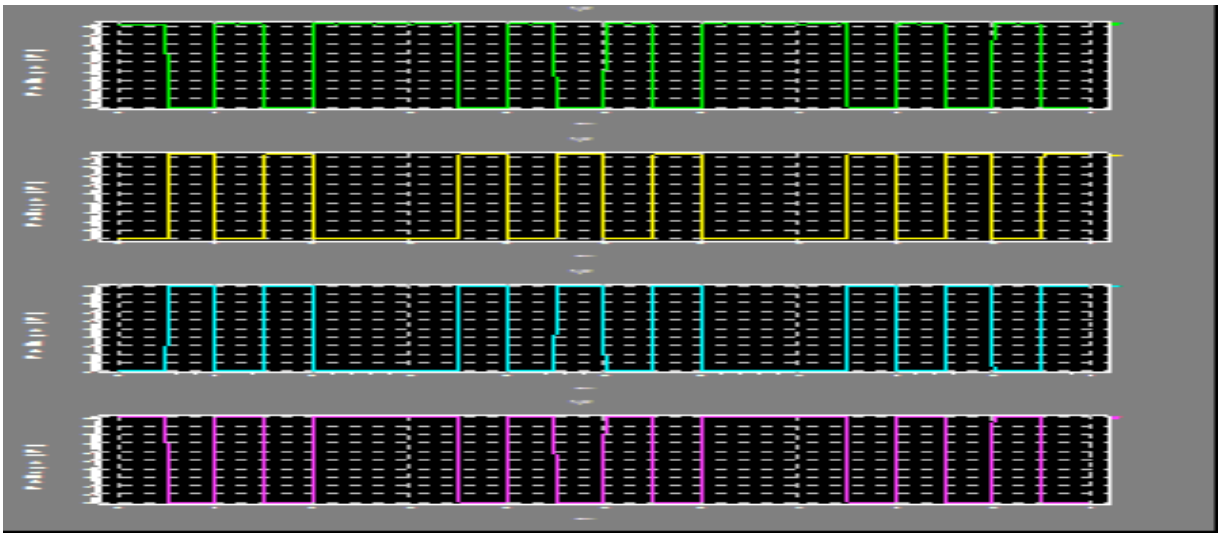

Fig. 6: Simulation of low power VCO in Digital (voltage versus Time)

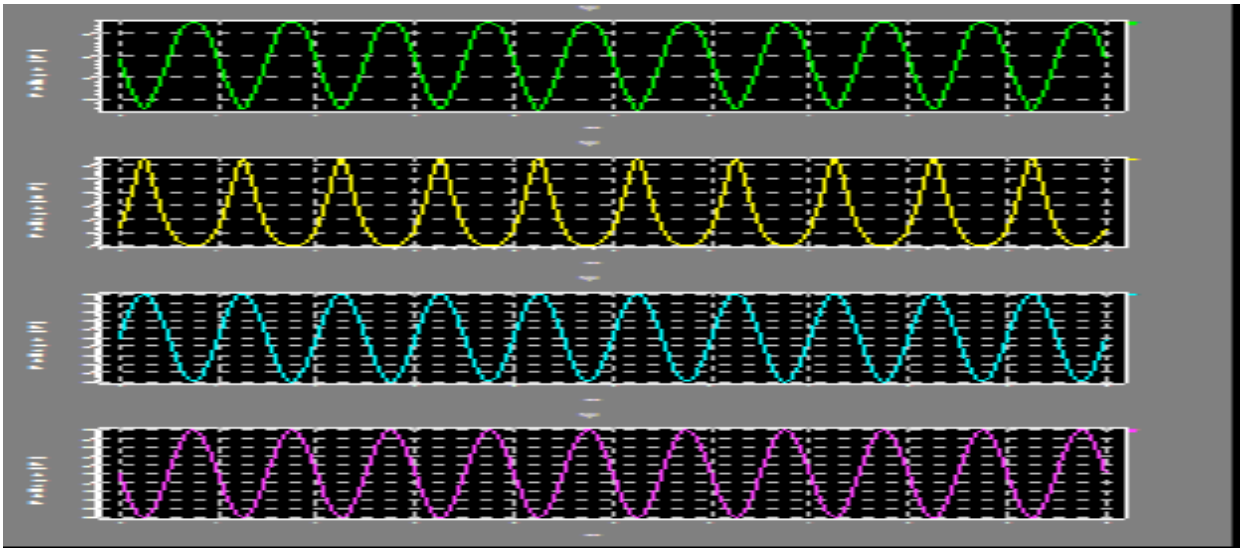

Fig. 7: Simulation of low power VCO in analog (voltage versus Time)

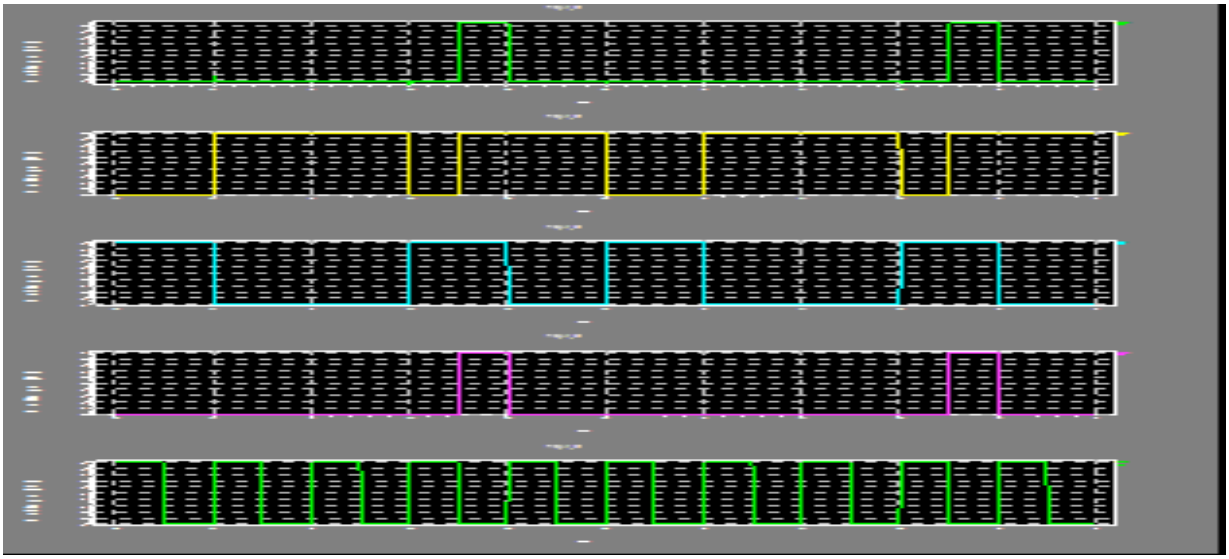

Fig. 8: Simulation of low power PFD in (Voltage versus Time)

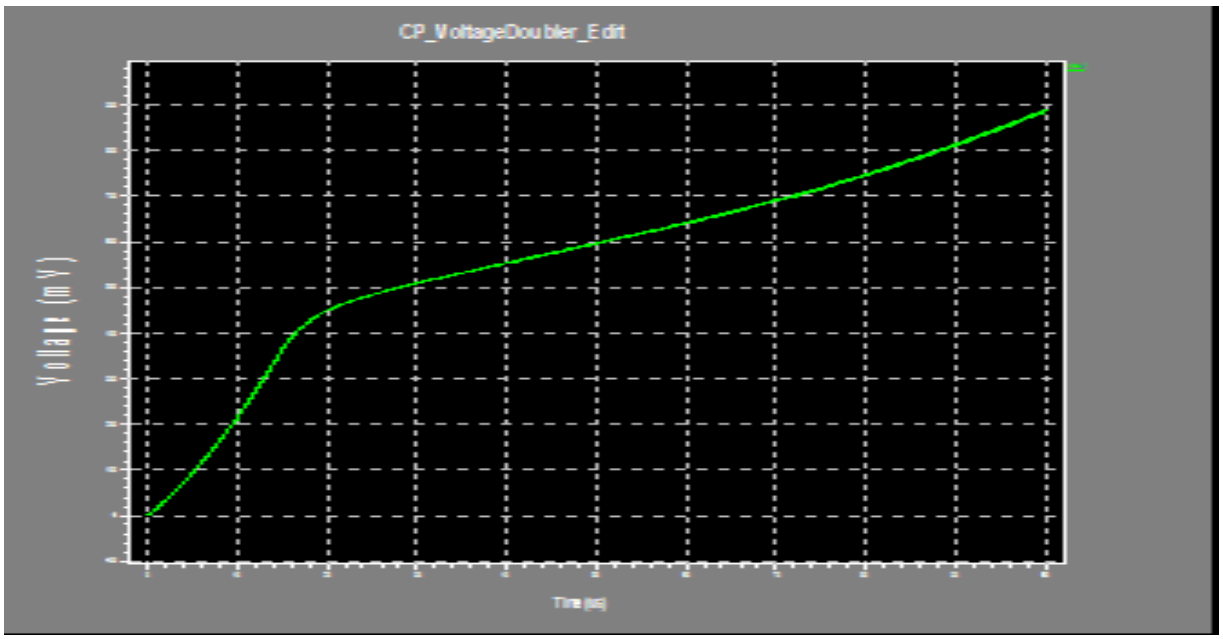

Fig.9: Simulation of low power PMOS Gate- controlled Voltage Doubler in (voltage versus Time)

VIII. CONCLUSION

The project is under progress. It is yet not completed and some of the block implementation are done. The VCO, charge pump and PFD are efficiently and effectively designed. The three modules are implemented on Tanner tool with good results.

REFERENCES

[1] Ms. Ujwala A. Belorkar 1 ,Dr. S.A. Ladhake 2 , "Design of Low Power Phase Locked Loop (PLL) Using 45 nm Technology ", International journal of VLSI design & communication systems(VLSIC), Vol.1,No.2June 2010.

[2] U. S. Patent Documents, Primary Examiner – Robert Pascal Assistant Examiner – Ryan Johnson, "Wide Range/High Speed Low Power Cmos VCO" Patent No: US7, 863, 991 B1, Jan.4, 2011.

[3] Adam Zaziabl "Low Power 1 GHz Charge Pump Phase-Locked Loop in 0.18 μm CMOS Process" MIXDES 2010, 17th International conference "Mixed Design of Integrated Circuits and Systems", June 24-26, 2010, Wroclaw, Poland.

[4] Ling Su and Dongsheng Ma "Design and Optimization of Integrated Low-Voltage Low - Monolithic CMOS Charge Pumps", International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM 2008

[5] Mansuri M., Liu D., Yang C., "Fast frequency acquisition phase frequency detectors for Gsamples/s phase-locked loops", IEEE Journal of Solid-State Circuits, 2002, vol. 37, pp. 1331 – 1334

[6] Razavi B., "Monolithic phase-locked loops and clock recovery circuits", IEEE Press, New York 1996

[7] Su, F.; Ki, W.H; Tsui, C.Y.: High efficiency cross-coupled doubler with no reversion loss. International Symposium on Circuits and Systems (ISCAS), May 2006, pp. 2761- 2764.

[8] Hung Q., Rogenmoser R.,"Speed optimization of edge-triggered CMOS circuit for gigahertz single-Phase clocks", IEEE Journal of Solid State Circuit, 1996, vol.31,pp 456- 465.